CLAIM LISTING

This listing of claims will replace all prior versions, and listings of claims in the application:

1-35 (Cancelled).

36. (New) An add-compare-select circuit, comprising:

an adder circuit to receive first and second sets of cost signals and configured to provide first and second summations of the first and second sets of cost signals;

a first synchronization circuit, coupled to the adder circuit, the first synchronization circuit configured to store and provide the first and second summations in synchrony with a clock signal;

a compare circuit to receive the first and second summations in response to the clock signal and configured to provide a comparison signal indicative of a relative difference between a magnitude of the first summation and a magnitude of the second summation;

a second synchronization circuit, coupled to the first synchronization circuit and the compare circuit, the second synchronization circuit configured to store and provide the first and second summations in synchrony with the clock signal and to store and provide the comparison signal in synchrony with the clock signal; and

a selection circuit, coupled to the second synchronization circuit, the selection circuit configured to provide a selected signal that is equal to one of the first or second summations in response to a value of the comparison signal.

37. (New) The add-compare-select circuit of Claim 36, wherein the adder circuit comprises:

a first adder unit coupled to receive a first previous cost signal and a first branch cost signal and configured to sum the first previous cost signal and the first branch cost signal to provide the first summation; and

a second adder unit coupled to receive a second previous cost signal and a second branch cost signal and configured to sum the second previous cost signal and the second branch cost signal to provide the second summation.

38. (New) The add-compare-select circuit of Claim 36, wherein the first synchronization circuit comprises:

a first register to receive the first summation and the clock signal, the first register configured to provide the first summation at an output of the first register in response to a first transition of the clock signal; and

a second register to receive the second summation and the clock signal, the second register configured to provide the second summation at an output of the second register in response to the first transition of the clock signal.

39. (New) The add-compare-select circuit of Claim 38, wherein the compare circuit provides the comparison signal having a first logic value in response to the magnitude of the first summation being larger than the magnitude of the second summation and provides the comparison signal having a second logic value in response to the magnitude of the first summation being smaller than the magnitude of the second summation.

40. (New) The add-compare-select circuit of Claim 39, wherein the second synchronization circuit comprises:

a third register to receive the first summation and the clock signal, the third register configured to provide the first summation at an output of the third register in response to a second transition of the clock signal;

a fourth register to receive the second summation and the clock signal, the fourth register configured to provide the second summation at an output of the fourth register in response to the second transition of the clock signal; and

a fifth register to receive the comparison signal and the clock signal, the fifth register configured to provide the comparison signal at an output of the fifth register in response to the second transition of the clock signal.

41. The add-compare-select circuit of Claim 40, further comprising a third synchronization circuit, coupled to the second synchronization circuit and the selection circuit, the third synchronization circuit configured to store and provide the selected signal in synchrony with the clock signal and to store and provide the comparison signal in synchrony with the clock signal.

42. (New) The add-compare-select circuit of Claim 41, wherein the third synchronization circuit comprises:

a sixth register to receive the selected signal and the clock signal, the sixth register configured to provide the selected signal at an output of the sixth register in response to a third transition of the clock signal; and

a seventh register to receive the comparison signal and the clock signal, the seventh register configured to provide the comparison signal at an output of the seventh register in response to the third transition of the clock signal.

43. (New) An add-compare-select circuit, comprising:

a first adder circuit to receive first and second sets of cost signals and configured to provide first and second summations of the first and second sets of cost signals;

a first synchronization circuit, coupled to the adder circuit, the first synchronization circuit configured to store and provide the first and second summations in synchrony with a clock signal;

a compare circuit to receive the first and second summations in response to the clock signal and configured to provide a first comparison signal indicative of a relative difference between a magnitude of the first summation and a magnitude of the second summation and further configured to provide a second comparison signal indicative of an actual difference between the magnitude of the first summation and the magnitude of the second summation;

a memory device to receive the second comparison signal and configured to provide an offset signal in response to the second comparison signal;

a selection circuit, coupled to the first synchronization circuit and the compare circuit, the selection circuit configured to provide a selected signal equal to one of the first or second summations in response to a value of the first comparison signal; and

a second synchronization circuit, coupled to the selection circuit and the memory device, the second synchronization circuit configured to store and provide the selected and offset signals in synchrony with the clock signal.

44. (New) The add-compare-select circuit of Claim 43, further comprising:

a second adder circuit to receive the selected signal and the offset signal and configured to provide a summation of the selected signal and the offset signal; and

a third synchronization circuit, coupled to the second adder circuit, the third synchronization circuit configured to store and provide the summation of the selected signal and the offset signal in synchrony with the clock signal.

45. (New) The add-compare-select circuit of Claim 43, wherein the adder circuit comprises:

a first adder unit to receive a first previous cost signal and a first branch cost signal and configured to sum the first previous cost signal and the first branch cost signal to provide the first summation; and

a second adder unit coupled to receive a second previous cost signal and a second branch cost signal and configured to sum the second previous cost signal and the second branch cost signal to provide the second summation.

46. (New) The add-compare-select circuit of Claim 43, wherein the first synchronization circuit comprises:

a first register to receive the first summation and the clock signal, the first register configured to provide the first summation at an output of the first register in response to a first transition of the clock signal; and

a second register to receive the second summation and the clock signal, the second register configured to provide the second summation at an output of the second register in response to the first transition of the clock signal.

47. (New) The add-compare-select circuit of Claim 46, wherein the compare circuit provides the first comparison signal having a first logic value in response to the magnitude of the first summation being larger than the magnitude of the second summation and provides the first comparison signal having a second logic value in response to the magnitude of the first summation being smaller than the magnitude of the second summation.

48. (New) The add-compare-select circuit of Claim 47, wherein the second synchronization circuit comprises:

a third register to receive the selected signal and the clock signal, the third register configured to provide the selected signal at an output of the third register in response to a second transition of the clock signal; and

a fourth register to receive the offset signal and the clock signal, the fourth register configured to provide the offset signal at an output of the fourth register in response to the second transition of the clock signal.

49. (New) An add-compare-select circuit, comprising:

a first synchronization circuit to receive first and second sets of cost signals and a clock signal, the first synchronization circuit configured to store and provide the first and second sets of cost signals in synchrony with the clock signal;

an adder circuit to receive the first and second sets of cost signals from the first synchronization circuit in response to the clock signal and configured to provide first and second summations of the first and second sets of cost signals;

a second synchronization circuit, coupled to the adder circuit, the second synchronization circuit configured to store and provide the first and second summations in synchrony with the clock signal;

a compare circuit to receive the first and second summations in response to the clock signal and configured to provide a comparison signal indicative of a relative difference between a magnitude of the first summation and a magnitude of the second summation;

a third synchronization circuit, coupled to the second synchronization circuit and the compare circuit, the third synchronization circuit configured to store and provide the first and second summations in synchrony with the clock signal and to store and provide the comparison signal in synchrony with the clock signal; and

a selection circuit, coupled to the third synchronization circuit, the selection circuit configured to provide a selected signal equal to one of the first or second summations in response to a value of the comparison signal.

50. (New) The add-compare-select circuit of Claim 49, wherein the first synchronization circuit comprises:

a first register to receive a first cost signal and the clock signal, the first register configured to provide the first cost signal at an output of the first register in response to a first transition of the clock signal;

a second register to receive a second cost signal and the clock signal, the second register configured to provide the second cost signal at an output of the second register in response to the first transition of the clock signal;

a third register to receive a third cost signal and the clock signal, the third register configured to provide the third cost signal at an output of the third register in response to the first transition of the clock signal; and

a fourth register to receive a fourth cost signal and the clock signal, the fourth register configured to provide the fourth cost signal at an output of the fourth register in response to the first transition of the clock signal.

51. (New) The add-compare-select circuit of Claim 50, wherein the adder circuit comprises:

a first adder unit to receive the first and second cost signals in response to the first transition of the clock signal and configured to sum the first and second cost signals to provide the first summation; and

a second adder unit to receive the third and fourth cost signals in response to the first transition of the clock signal and configured to sum the third and fourth cost signals to provide the second summation.

52. (New) The add-compare-select circuit of Claim 51, wherein the second synchronization circuit comprises:

a fifth register to receive the first summation and the clock signal, the fifth register configured to provide the first summation at an output of the fifth register in response to a second transition of the clock signal; and

a sixth register to receive the second summation and the clock signal, the sixth register configured to provide the second summation at an output of the sixth register in response to the second transition of the clock signal.

53. (New) The add-compare-select circuit of Claim 52, wherein the fifth register includes a shift register.

54. (New) The add-compare-select circuit of Claim 52, wherein the sixth register includes a shift register.

55. (New) The add-compare-select circuit of Claim 52, wherein the compare circuit provides the comparison signal having a first logic value in response to the magnitude of the first summation being larger than the magnitude of the second summation and provides the comparison signal having a second logic value in response to the magnitude of the first summation being smaller than the magnitude of the second summation.

56. (New) The add-compare-select circuit of Claim 55, wherein the third synchronization circuit comprises:

a seventh register to receive the first summation from the fifth register and coupled to receive the clock signal, the seventh register configured to provide the first summation at an output of the seventh register in response to a third transition of the clock signal;

an eighth register to receive the second summation from the sixth register and to receive the clock signal, the eighth register configured to provide the second summation at an output of the eighth register in response to the third transition of the clock signal; and

a ninth register to receive the comparison signal and the clock signal, the ninth register configured to provide the comparison signal at an output of the ninth register in response to the third transition of the clock signal.

57. (New) The add-compare-select circuit of Claim 56, further comprising a fourth synchronization circuit comprises:

a tenth register to receive the selected signal and the clock signal, the tenth register configured to provide the selected signal at an output of the tenth register in response to a fourth transition of the clock signal; and

an eleventh register to receive the comparison signal and the clock signal, the eleventh register configured to provide the comparison signal at an output of the eleventh register in response to the fourth transition of the clock signal.